Reg No.:_____ Name:_____

0520MCA103122001

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

First Semester MCA (2 Years) Degree Examination December 2020

Course Code: 20MCA103

Course Name: DIGITAL FUNDAMENTALS & COMPUTER ARCHITECTURE

Max. Marks: 60 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1	Represent -45 in sign magnitude, 1's complement and 2's complement form.	(3)
2	Implement a Full adder by deriving expressions from its truth table.	(3)
3	Implement a JK flip flop and explain its working.	(3)
4	Construct a Mod-5 Asynchronous Counter.	(3)
5	Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much?	(3)
6	Briefly describe the 5 key components of a Computer System.	(3)
7	What are the MIPS Datapath components required to construct a Branch (beq) Datapath? Represent their symbols and the control signals associated with them.	(3)
8	Briefly explain the different types of Pipeline hazards.	(3)
9	Define Temporal locality and Spatial locality.	(3)
10	What is a Semi-conductor Memory?	(3)

PART B

Answer any one question from each module. Each question carries 6 marks.

Module I

11	Minimize the Boolean expression $f(A,B,C,D)=\Sigma m(1,5,6,7,9,15)+d(2,3,11,13)$ using Karnaugh map and realize it using Logic gates.	(6)

OR

12	Convert the decimal number 3.257 * 10^4 into IEEE-754 Single Precision Floating Point binary representation.	(6)

Module II

13 Construct a 3-bit Up/Down Synchronous Counter. Show the relevant Boolean expressions. (6)

OR

14 Implement and explain the working of a 4-bit Parallel-In Serial-Out [PISO] Shifter. (6)

Module III

15 List down and briefly explain the 8 great ideas in Computer Architecture. (6)

OR

16 Define Addressing mode. Explain 5 Addressing modes with examples. (6)

Module IV

17 Draw the Single Cycle Datapath for implementing Memory Reference instructions and R-Format instructions. (6)

OR

18 Write notes on: Direct Memory Access & Interrupt Handling. (6)

Module V

19 Explain the various Cache Mapping Techniques. (6)

OR

20 a) Construct a 1KB Memory IC using 1024x4 Memory chips. (4)

b) What do you understand by Virtual Memory? (2)

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